Claims:

1. An analog-to-digital converter comprising:

a converter input for receiving an analog input signal to be converted;

an input impedance network for creating a plurality of reference signals;

a plurality of comparators corresponding to said plurality of reference signals, each of said comparators having a first comparator input connected to said input impedance network to provide said comparator with one of said plurality of reference signals, a second comparator input connected to said converter input for receiving said analog input signal, a third comparator input connected to its own enabling signal source for receiving an enabling signal, and a comparator output that outputs a signal only when signals are received at the same time at the first, second, and third comparator inputs; and

a converter output connected to a comparator output of each of said plurality of comparators.

2. An analog-to-digital converter as claimed in claim 1, wherein the first comparator input and second comparator input of each of said plurality of comparators control the transfer of an enabling signal at the third comparator input to a signal at the comparator output, and wherein the transfer characteristic of each comparator between the third comparator input to the comparator output is linear.

3. An analog-to-digital converter as claimed in claim 2 wherein each of said plurality of comparators comprises a first and a second three-terminal semiconductor device, said first semiconductor device having its base or gate connected to said first comparator input and said second semiconductor device having its base or gate connected to said second comparator input, and the low impedance connection of said first and second semiconductor devices connected in common to said third comparator input.

4. An analog-to-digital converter as claimed in claim 3 wherein each of said first and second semiconductor devices is a field-effect transistor device.

5. An analog-to-digital converter as claimed in claim 3 wherein each of said first and second semiconductor devices is a bipolar junction transistor device.

6. An analog-to-digital converter comprising:

a converter input for receiving an analog input signal to be converted;

an input impedance network connected to said converter input for creating a plurality of reference signals having a parabolic profile, said profile having a zero which varies as a function of said analog input signal;

a plurality of comparators corresponding to said plurality of reference signals, each of said comparators having a first comparator input connected to said input impedance network to provide said comparator with one of said plurality of reference signals, a second comparator input connected to said input impedance network to provide said comparator with a different one of said plurality of reference signals, a third comparator input connected to its own enabling signal source for receiving an enabling signal, and a comparator output that outputs a signal only when signals are received at the same time at the first, second, and third comparator inputs; and

a converter output connected to a comparator output of each of said plurality of comparators.

7. An analog-to-digital converter as claimed in claim 6, wherein the first comparator input and second comparator input of each of said plurality of comparators control the transfer of an enabling signal at the third comparator input to a signal at the comparator output, and wherein the transfer characteristic of each comparator between the third comparator input to the comparator output is linear.

8. An analog-to-digital converter as claimed in claim 7 wherein each of said plurality of comparators comprises a first and a second three-terminal semiconductor device, said first semiconductor device having its base or gate connected to said first comparator input and said second semiconductor device having its base or gate connected to said second comparator input, and the low impedance connection of said first and second semiconductor devices connected in common to said third comparator input.

9. An analog-to-digital converter as claimed in claim 8 wherein each of said first and second semiconductor devices is a field-effect transistor device.

10. An analog-to-digital converter as claimed in claim 8 wherein each of said first and second semiconductor devices is a bipolar junction transistor device.

11. An analog-to-digital converter as claimed in claim 6 wherein said analog input signal is a differential signal applied across said impedance network.

12. A method for converting an analog input signal into a digital output signal, comprising:

providing a converter having an input for receiving an analog input signal and a plurality of comparators for comparing said analog input signal directly or indirectly to a plurality of reference signals;

providing a plurality of reference signals corresponding to each of said plurality of comparators;

applying an analog input signal to said converter;

repeatedly, in a successive approximation manner, selectively enabling or disabling each of said plurality of comparators to compare said signals and then summing the outputs of said comparators together; and

producing said digital output signal from said summed outputs of said comparators.

13. A method as claimed in claim 12 further comprising creating a virtual comparator during an iteration of said repeated comparisons in a successive approximation manner by enabling more than one of said plurality of comparators at the same time and modifying the outputs of said enabled comparators prior to summing said outputs together, such modifications in proportions that linearly interpolate between the outputs of said enabled comparators so as to simulate a virtual comparator having an interstitial output between the outputs of said enabled comparators.

14. A method as claimed in claim 12 wherein said analog input signal is differential.

15. An analog-to-digital converter comprising:

a converter input for receiving an analog input signal to be converted to digital data;

a parabolic impedance network, the network including a bank of resistors, a plurality of nodes occurring between each resistor a plurality of current sources, where each current source corresponds to each node, wherein each resistor and corresponding current source is configured to create an individual voltage reference having a value that occurs in a parabolic manner in relation to other voltage references occurring across the impedance network;

a plurality of comparators corresponding to said plurality of reference signals, wherein the parabolic impedance network provides parabolic reference voltage inputs summed together with an input voltage to an input of each corresponding comparator, wherein each comparator includes an enablement signal input connected to an enabling signal source for receiving an enabling signal, and a comparator output that outputs a signal when the comparator is enabled; and

a converter output connected to a common output of each of said plurality of comparators, wherein the output is configured to output a value that is interpolated between two nodes to create a virtual comparator occurring between two nodes.

16. A voltage to current converter according to Claim 15, wherein the converter output connected to a common output of each of said plurality of comparators is configured to output a value that is interpolated between two nodes according to the formula $V_{i,out} = V_i \cdot E_i$, where $1 \leq i \leq N$, V_i is the difference between the input signal V_{in} and the reference signal applied to comparator C_i, and E_i is the value of an enabling signal that can be varied between two consecutive integers to create a virtual comparator occurring between two nodes.

17. A voltage to current converter according to Claim 15, wherein the parabolic impedance network is configured to provide a reference voltage to the an input of a comparator of each of the plurality of comparators in a manner that would produce reference voltages in a parabolic manner, where the reference voltage provided to one comparator is of a relatively lower value than the reference voltage provided to an intermediately located comparator, and where the reference voltage of the intermediately located comparator receives a maximum voltage value relative to the other comparators.

18. A voltage to current converter according to Claim 15, wherein the

parabolic impedance network is configured to provide a reference voltage to the an input of a comparator of each of the plurality of comparators in a manner that would produce reference voltages in a parabolic manner, where the reference voltage provided to one comparator is of a relatively higher value than the reference voltage provided to an intermediately located comparator, and where the reference voltage of the intermediately located comparator receives a minimum voltage value relative to the other comparators.

19. A voltage to current converter according to Claim 15, wherein the comparators each include a pair of transistors, wherein the parabolic impedance network is configured to provide a reference voltage to the drain of one of a pair of transistors of each of the plurality of comparators in a manner that would produce reference voltages in a parabolic manner, where the reference voltage provided to one comparator is of a relatively higher value than the reference voltage provided to an intermediate comparator, and where the intermediate comparator receives of a minimum voltage value relative to the other comparators.